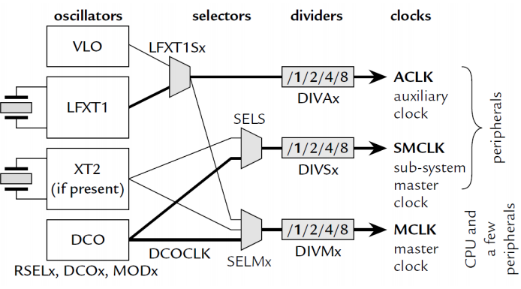
Generic Definitions:

- MPU: Micro Processor Unit

- MCU: Micro Controller Unit

- SoC: System on a Chip

- SFR: Special Function Register

- GPR: General Purpose Register

- DCO: Digitally Controlled Oscillator

- VLO: Very Low-power Oscillator

- ACLK: Auxiliary Clock

- SMCLK: Sub-system Master Clock

- MCLK: Master Clock

- ISR: Interrupt Service Routine

- IRQ: Interrupt Request

- PC: Program Counter

- SP: Stack Pointer

- SR: Status Register

- PUC: Power Up Clear

- LPM: Low Power Mode

- ADC: Analog to Digital Converter

- GPIO: General Purpose Input Output

- RISC: Reduced Instruction Set Comp.

- ISA: Instruction Set Architecture

- AM: Active Mode

- GIE: Global Interrupt Enable

- SAR: Successive Approximation Register

MSP430 Architecture:

- 16b addr bus -> 64KB addr space

- 1KB RAM

- 32KB Flash

- Memory Mapped IO:

- Little Endian bit & byte ordering

- Not RISC ISA:

1. All Arith. & Logical Instrucs are Register-to-- . . . Register (No)

- MSP430 ALU ops can use any addressing mode

2. Single Cycle Instruction Execution (Yes)

- The ALU itself only needs 1 cycle per operation

3. A Few Simple Instruction Formats (No)

- MSP430 Opcode has variable length (3, 4, 9 b)

- Imms & Addrs may extend into 2nd or 3rd word

4. A Few Simple Addressing Modes (No)

- Some MSP430 addr modes go back for 2nd mem word

- Inhibits single-cycle address calculation

- SR: [C = Carry, Z = Zero, N = Negative, V = Overflow]

- DCO: @ PUC = 1.15 MHz, Config up to 16MHz

- VLO: 12 KHz +- A lot

Embedded C:

- extern: Defined with global scope in 1 file & . . . . . referenced in another

- volatile: when something changes value w/o comp knowing

- turns off optimization for that variable

- static: once declared the variable never deleted

- Do not use Dynamic Mem Allocation or Recursion, embedded systems have a limited amount of RAM

- Pragmas:

- Implementation-specific directive to the compiler

- Place following code at specific address

- Log that address in IRQ Vector word

- Intrinsic function:

- C function that manipulates a specific h-ware unit

- Processor dependent

GPIO:

- 4 8b GPIO ports – Px.n – x{1..4} – n{0..7}

- IE & Triggering Edge Detection on P1 & P2 only

- PxDIR – 0 = in, 1 = out

- PxIN - 1 = high, 0 = low

- PxOUT – 1 = high, 0 = low

- PxREN – 1 = enab, 0 = dis & PxOUT – 1 = PullUp

\*Interrupts = GIE bit is set in SR to work

- PxIE – 0 = disabled

- PxIES – 0 = rising edge

- PxIFG – must be cleared by S-ware

- EX: P1IFG &= ~0x04; // clears P1.2 IFG

LPMs:

- Easy to get in and out of:

- H-Ware wakes to AM in interrupt (SR = 0x0000)

- ISR can write to old value of SR stored on stack

- Changes mode of MCU on exit of ISR

- H-Ware Actions on ISR

- Push PC & SR (16b words) onto the Stack & clear SR

- SR = 0x0000 -> AM & GIE disabled

- Pop PC & SR off stack – restore program state

- bic = bit clear

- bis = bit set

- Writing a ISR:

#pragma vector = IRQ\_VECTOR\_NAME

\_\_interrupt void NameOfISR(void)

Timers:

- Contents:

- 1 Timer block w/ counter register (TAR, max=0xFFFF)

- 3 Capture Compare Channels

- Interrupts:

- CCIFG0 has its own IRQ vector (TACCR0) (auto clear)

- Others in TxIV vector register (manually clear)

- Timer Block Counting Modes:

- Continuous:

- TAR counts up to 0xFFFF (no IRQ @ max val)

- Rollover to 0 -> TAIFG

- Period = 2^16 = 64K TACLK cycles

- Up:

- TAR counts up to TACCR0

- Then rolls over to 0 -> TAIFG

- Period = TACCR0 + 1

- Up/Down:

- TAR counts up to TACCR0

- Then back down to 0

- Period = 2 \* TACCR0

- Compare Mode:

- TACCRx is preloaded with a value.

- Triggered when TAR == TACCRx

- Synchronous Capture:

- TA can synch input to falling clock edge

- TAR value changes on rising edge

- Avoids capturing transient values of TAR

- IDx: Internal Divider Bits

- 00 = 1, 01 = 2, 10 = 4, 11 = 8 (2^x = div)

- \_\_even\_in\_range(Value, Limit):

- Value is guaranteed to be even

- Value is bounded by a max of Limit

- PWM:

- Analog Voltage proportional to PW/PD

Brushed DC Motors:

- Basic Physics:

- Alignment of 2 magnetic fields

- Commutation: The act of reversing a field

- Commutators: Rotating, conductive slip ring mounted

Mounted on the shaft.

- Multi-winding Rotors:

- Smoother torque 2 windings - 90ͦ offset

- Greater average torque 3 windings - 60ͦ offset

- Performance Parameters:

- RPM vs Current – Max current @ 0 RPM

- RPM vs Back EMF – Max Back EMF @ Max RPM

- Motor as a generator:

- force shaft to rotate faster than no-load speed

- Back EMF > Vin

- Command & Control:

- Speed controlled via PWM

- Direction controlled via H-Bridge

Servo Motors:

- Components:

- Motor, Gear box, Position sensor, Error Amp, &

Pulse width to voltage converter (Low Pass Filter)

- PD = 20 ms (50 Hz)

- PW range (1.0 ms, 2.0 ms)

ADC:

- Issues with SAR ADCs:

- ADC can only convert one channel at a time

- Can only measure relative voltage

- Multiplexed SAR’s

- Every switch of inputs starts new conversion

- wait for sample hold time

- n-bit conversion delay

- Clock Frequency:

- SAR evaluates 1 bit per clock cycle

- Clock can’t be too fast

- Can’t be too slow either:

- Caps leak & comp amp draws current

- ACLK is too slow

- Generating Stable Reference Voltage:

- Vref source sees differing loads as MCU switches

states.

- Must be stable

A screenshot of a cell phone

Description automatically generated

- Calculating NADC:

- NADC = 1023((Vin – VR-)/(VR+-VR-))

- Upper Lim = VR+ , Vin >= VR+ , NADC = 0x03FF

- Lower Lim = VR- , Vin <= VR1 , NADC = 0x0000

- Greater than 200 ksps max conversion rate

- Monotonic conversion

- No missing codes

- Gray bits mod only when ENC == 0

Brushless Motors:

- Rotor is permanent magnet

- Commutate the stator field electronically

Stepper Motors:

- Rotate stator field in discrete steps

- Rotation achieved by switching stator windings

on & off in proper sequence

- Different Types:

- Variable Reluctance:

- Rotor is ferromagnetic core with teeth

- No H-Bridge required

- Unipolar:

- Rotor is permanent magnet

- Center tap in each coil

- Easy switch field directions

- No H-Bridge required

- Bipolar:

- Not center tapped

- Fields reversed by switching PWR & GND on both

ends

A picture containing object

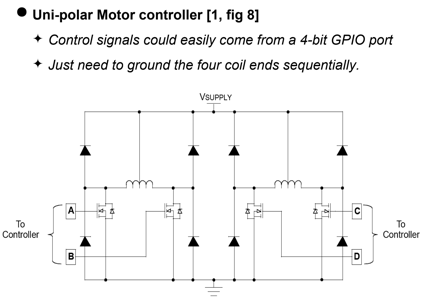
Description automatically generated - H-Bridge required (1 / field winding)

A close up of a clock

Description automatically generatedA close up of text on a white background

Description automatically generatedA picture containing object

Description automatically generatedA close up of a clock

Description automatically generatedA close up of a map

Description automatically generated